Neutral Point Clamped MOSFET Inverter With Full-Bridge Configuration for Nonisolated Grid-Tied Photovoltaic System

Chakravartula Anandababu, *Student Member, IEEE*, and Baylon G. Fernandes, *Member, IEEE*

***Abstract*— Existing nonisolated full-bridge neutral point clamped (NPC) inverters for a single-phase grid-tied photovoltaic (PV) system have limitations such as shoot-through and low European Union (EU) efficiency. In order to address these limitations, an NPC superjunction MOSFET nonisolated inverter with full-bridge configuration (NIIFBC) is proposed in this paper. This inverter reduces the possibility of shoot-through, thereby improving the reliability of the grid-tied PV system. It controls the grid current by energizing two coupled inductors individually during positive and negative half-grid cycles. This obviates the possibility of reverse recovery loss in switches due to their body diodes. Furthermore, two external silicon carbide diodes of a clamping branch cause negligible reverse recovery loss in switches besides a constant common-mode voltage. Therefore, the main claims of NIIFBC are low leakage current, high EU efficiency, and reliability. A generalized leakage current model for the proposed inverter is developed. In order to validate the veracity of the model and the claims of NIIFBC, a 1-kW prototype is designed and developed. The experimental results of NIIFBC validate the claims made by the authors. Its performance comparison with the existing nonisolated full-bridge inverters is given. Furthermore, a variant circuit of NIIFBC operating at nonunity power factor is proposed.**

***Index Terms*— Common-mode voltage (CMV), grid-tied photovoltaic (PV) system, leakage current, nonisolated inverter, superjunction MOSFET.**

I. Introduction

GREEN energy sources such as solar and wind are being used to fulfill the constantly increasing demand for electrical energy. The contemporary developments in photovoltaic (PV) cell technologies and power electronic (PE) devices make solar electrical power generation popular, especially in the grid-tied sector [1]. The PV source and the grid are interfaced using PE converters [2]–[6]. Their initial cost is lower than that of the PV panels. However, the energy yield of a grid-tied PV system depends on the reliability and the efficiency of PE converters.

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A single-stage nonisolated inverter makes the grid-tied PV system more efficient and reliable than that with isolation [7], [8]. However, in this circuit, there is a path for leakage current through the inverter and grid and stray capacitors between PV terminals to the ground [9], [10]. A high-frequency voltage across the PV stray capacitors results in substantial leakage current. It causes a deterioration in the quality of the grid current, electromagnetic interference, and, eventually, disconnection of the PV source from the grid [11].

A low-frequency sinusoidal voltage across the PV stray capacitors besides a constant common-mode voltage (CMV) is essential to reduce the leakage current [12]. Such requirements are fulfilled when the single-phase full-bridge inverter is controlled using bipolar sinusoidal pulsewidth modulation (SPWM) technique [13]. Use of this modulation technique results in high switching loss and requires large filter inductor compared with unipolar and hybrid SPWM techniques. When these techniques are used, the voltage profile across the PV stray capacitors is either a pulsewidth modulated or a square wave of grid frequency [14]. Such voltages cause substantial and moderate leakage currents, respectively. If the source is disconnected from the grid during freewheeling modes of operation, these SPWM techniques can attain a dc level shifted grid voltage across the PV stray capacitors [15], [19], [22].

A nonisolated inverter that achieves isolation on the dc side using an additional switch is reported in [15]. The body diode of a switch in its freewheeling path is active during positive and negative half-grid cycles. If superjunction MOSFET devices are used, the conduction of their body diodes leads to high reverse recovery switching loss. On the other hand, use of an insulated gate bipolar transistor (IGBT) device results in low EU efficiency as the power loss due to its fixed ON-state voltage drop is predominant at light loads. Such a power loss is absent in superjunction MOSFET devices and they have low ON-state resistance characteristics. The superjunction MOSFET nonisolated inverters having high EU efficiency are reported in [19]–[21]. Nevertheless, in these inverters, there is a possibility of shoot-through because of their synchronous buck structure. Such a limitation is addressed in an asynchronous voltage source inverter, which improves the reliability of the grid-tied PV system [22]. Despite their high EU efficiency and/or high reliability, the nonisolated superjunction MOSFET inverters do not maintain CMV at a constant value and therefore have high leakage current [19]–[22]. In addition, the leakage current due to the CMV of nonconducting paths and

the circuit operation at nonunity power factor (non-UPF) are not analyzed.

On the other hand, the CMV remains constant in the case of neutral point clamped (NPC) nonisolated inverters [23]–[28]. A split inductor NPC inverter that is derived from the dual-buck half-bridge inverter is presented in [23]. This inverter has lowest device count and reduces the possibility of shoot-through, which improves the reliability. The other nonisolated half-bridge inverter with fewer switches is presented in [24]. However, the half-bridge NPC topologies require twice the input voltage compared with full-bridge, for the given root-mean-square (rms) value of the ac output voltage. This necessitates a dedicated dc–dc boost stage or a large number of series-connected PV panels at the input.

An optimized full-bridge NPC (oH5) nonisolated inverter having lowest device count is proposed in [25]. In this inverter, the CMV does not remain constant, which is maintained at a constant value in H-bridge zero-voltage rectifier inverter [26]. In addition, there is a possibility of shoot-through across the dc link in these inverters. The full-bridge dc bypass (FBDCBP) and a family of NPC inverter topologies do not have the possibility of such shoot-through and have low leakage current characteristics [27], [28]. However, there could be a phase leg shoot-through due to the malfunctioning of gate drive circuits. Such a limitation exists in all the state-of-the-art nonisolated full-bridge NPC inverters. Their EU efficiency is poor because they use IGBT devices as a main switch to realize the circuit. Therefore, the full-bridge NPC nonisolated inverters increase the payback period and reduce the reliability of the grid-tied PV system.

In order to design a grid-tied PV system having low payback period and high reliability, an NPC superjunction MOSFET nonisolated inverter with full-bridge configuration (NIIFBC) is proposed in this paper. It has the following features:

1) a constant CMV and low leakage current characteristics;
2) reduces the possibility of shoot-through at switching frequency as well as at zero crossings of the grid voltage thereby improving the system reliability;
3) no reverse recovery loss in main switches;
4) high EU efficiency;
5) a compact design as increment in the respective power loss at higher switching frequencies is very low.

This paper is organized as follows. In Section II, a generalized leakage current model for nonisolated single-phase full-bridge inverter is presented, as the existing models do not yield an innate relation among leakage current, grid voltage and CMV. The modes of operation and the low leakage current feature of NIIFBC that is controlled using the hybrid SPWM technique are presented in Section III. Section IV presents the simulation and the experimental results of NIIFBC operating at unity power factor (UPF). Its performance comparison with the state-of-the-art nonisolated inverter topologies is presented in Section V. A variant circuit of NIIFBC for nonUPF operation is also presented. The elicited conclusions are summarized in Section VI.

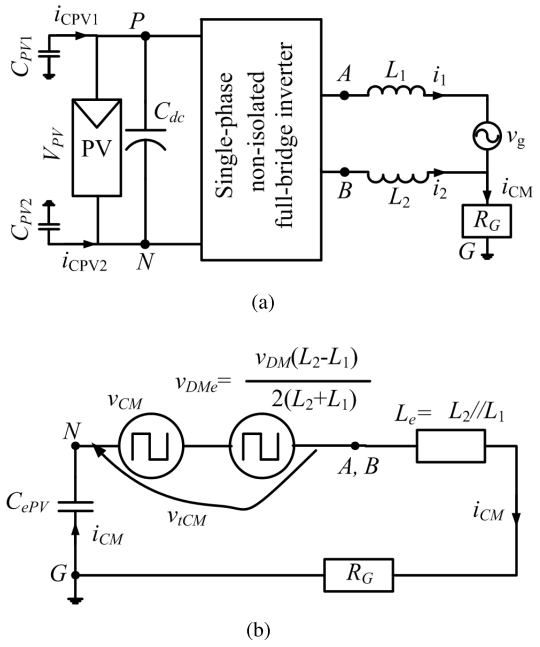


Fig. 1. (a) Generalized single-phase nonisolated full-bridge PV inverter. (b) Switching frequency leakage current model of the generalized nonisolated PV inverter [29].

II. Generalized Leakage Current Model of Nonisolated Single-Phase Full-Bridge Inverter

A generalized single-phase nonisolated full-bridge grid-tied PV inverter is shown in Fig. 1(a). It is considered in order to formulate the analytical relationship among the CMV, the leakage current, and the voltages across PV stray capacitors. An equivalent leakage current model at switching frequency is derived in [29] and shown in Fig. 1(b). The CMV in terms of node voltages A and B to N is given by

$$v_{\mathrm{tCM}} = v_{\mathrm{CM}} + (v_{\mathrm{AN}} - v_{\mathrm{BN}})\frac{L_2 - L_1}{2(L_2 + L_1)} \tag{1}$$

where L_1 and L_2 are filter inductors and $v_{\mathrm{CM}} = ((v_{\mathrm{AN}} + v_{\mathrm{BN}})/2)$. It is evident from Fig. 1(b) that a constant v_{tCM} is necessary to mitigate the leakage current. However, this is an implicit way of arriving at the relationship between v_{tCM} and the leakage current. Furthermore, the leakage current due to grid voltage is not taken into account. The effect of grid voltage on the leakage current is analyzed in [30]. However, this study does not present an innate relationship among the CMV, the grid voltage, and the leakage current.

In this paper, the instantaneous analytical relationships between v_{CM} and the voltages of PV stray capacitors are formulated. Subsequently, a relationship between v_{CM} and the leakage current is obtained. From Fig. 1(a), the leakage current, i_{CM} is given by

$$i_{\mathrm{CM}} = i_1 + i_2 \tag{2}$$

where i_1 and i_2 are the currents flowing through L_1 and L_2, respectively. The differential mode current i_{DM} is given as

$$i_{\mathrm{DM}} = \frac{i_1 - i_2}{2}. \tag{3}$$

Solving (2) and (3), i_1 and i_2 are given as

$$i_1 = i_{\mathrm{DM}} + \frac{i_{\mathrm{CM}}}{2} \tag{4}$$

$$i_2 = -i_{\mathrm{DM}} + \frac{i_{\mathrm{CM}}}{2}. \tag{5}$$

The analytical relationship between i_{DM} and v_{DM} using mesh analysis is given by

$$\frac{di_{\mathrm{DM}}}{dt} = \frac{v_{\mathrm{DM}} - v_g}{L_1 + L_2} + \frac{L_2 - L_1}{2(L_1 + L_2)}\left(\frac{di_{\mathrm{CM}}}{dt}\right) \tag{6}$$

where v_g is the grid voltage. v_{PG} and v_{NG} are the voltages across the PV stray capacitors C_{PV1} and C_{PV2}, respectively. The relationship between them is given by

$$v_{\mathrm{PN}} = v_{\mathrm{PG}} - v_{\mathrm{NG}} = V_{\mathrm{PV}}. \tag{7}$$

where v_{PA} and v_{NA} are the voltages at nodes P and N to A, respectively. The relationship between v_{PA} and v_{NA} is given by

$$v_{\mathrm{PN}} = v_{\mathrm{PA}} - v_{\mathrm{NA}} = V_{\mathrm{PV}}. \tag{8}$$

The voltages across C_{PV1} and C_{PV2} can be found using mesh analysis as

$$v_{\mathrm{PG}} = v_{\mathrm{PA}} + L_1\frac{di_1}{dt} + v_g + i_{\mathrm{CM}}R_G \tag{9}$$

$$v_{\mathrm{NG}} = v_{NB} + L_2\frac{di_2}{dt} + i_{\mathrm{CM}}R_G \tag{10}$$

where R_G is the ground resistance. v_{PG} can be represented in terms of v_{AN} and v_{BN} by substituting (7) and (8) in (10) and (9), respectively, as

$$v_{\mathrm{PG}} = V_{\mathrm{PV}} - v_{\mathrm{AN}} + L_1\frac{di_1}{dt} + v_g + i_{\mathrm{CM}}R_G \tag{11}$$

$$v_{\mathrm{PG}} = V_{\mathrm{PV}} - v_{\mathrm{BN}} + L_2\frac{di_2}{dt} + i_{\mathrm{CM}}R_G. \tag{12}$$

Adding (11) and (12) and substituting (4)–(6), the analytical relation for the voltage across PV stray capacitor C_{PV1} is derived as

$$v_{\mathrm{PG}} = V_{\mathrm{PV}} - v_{\mathrm{tCM}} + \frac{L_2}{L_1 + L_2}(v_g) + \frac{L_1L_2}{L_1 + L_2}\frac{di_{\mathrm{CM}}}{dt} + i_{\mathrm{CM}}R_G. \tag{13}$$

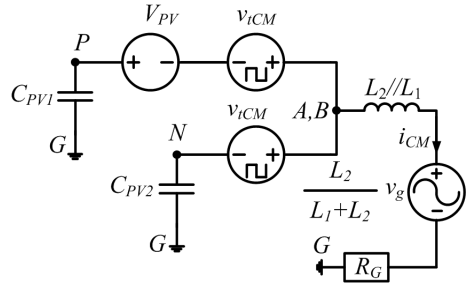
Further, the instantaneous relationship between the voltage across PV stray capacitor C_{PV2} and v_{tCM} can be obtained by substituting (7) in (13) as

$$v_{\mathrm{NG}} = -v_{\mathrm{tCM}} + \frac{L_2}{L_1 + L_2}(v_g) + \frac{L_1L_2}{L_1 + L_2}\frac{di_{\mathrm{CM}}}{dt} + i_{\mathrm{CM}}R_G. \tag{14}$$

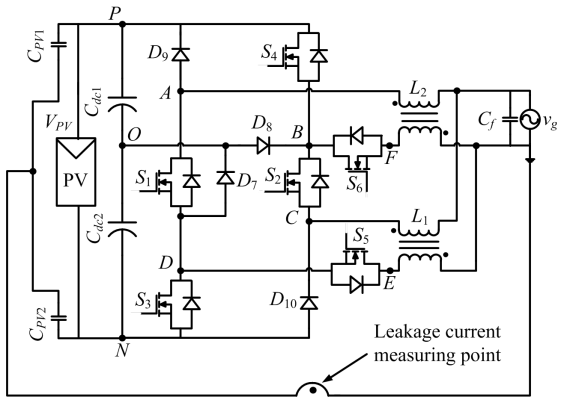
A modified leakage current model for the generalized nonisolated PV inverter that is based on (13) and (14) is shown in Fig. 2(a). When L_1 and L_2 are equal, the simplified form of (13) and that of (14) are given, respectively, as

$$v_{\mathrm{PG}} = V_{\mathrm{PV}} - v_{\mathrm{CM}} + \frac{v_g}{2} + \frac{L_1}{2}\frac{di_{\mathrm{CM}}}{dt} + i_{\mathrm{CM}}R_G \tag{15}$$

$$v_{\mathrm{NG}} = -v_{\mathrm{CM}} + \frac{v_g}{2} + \frac{L_1}{2}\frac{di_{\mathrm{CM}}}{dt} + i_{\mathrm{CM}}R_G. \tag{16}$$



(a)



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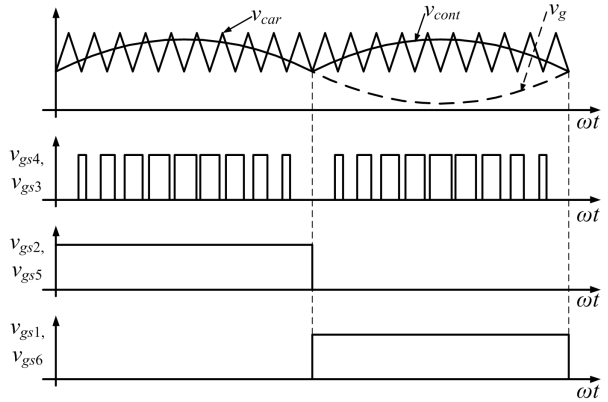

(c)

Fig. 2. (a) Modified leakage current model of the generalized nonisolated full-bridge PV inverter. (b) Power stage of the single-phase NIIFBC. (c) Hybrid SPWM switching strategy for NIIFBC operating at UPF.

In order to simplify the analysis, the voltage drop due to i_{CM} is neglected in (15) and (16). Therefore, the relationship between i_{CM} and v_{CM} can be expressed as

$$i_{\mathrm{CM}} = C_{\mathrm{PV1}}\frac{dv_{\mathrm{PG}}}{dt} + C_{\mathrm{PV2}}\frac{dv_{\mathrm{NG}}}{dt}; \quad C_{\mathrm{PV1}} = C_{\mathrm{PV2}}$$

$$i_{\mathrm{CM}} = C_{\mathrm{PV1}}\frac{d(V_{\mathrm{PV}} - 2v_{\mathrm{CM}} + v_g)}{dt}. \tag{17}$$

It is evident from (17) that the i_{CM} is profiled by v_{CM} and v_g. If v_{CM} is maintained at a constant value of $(V_{\mathrm{PV}}/2)$, the leakage current depends on the grid voltage magnitude and frequency.

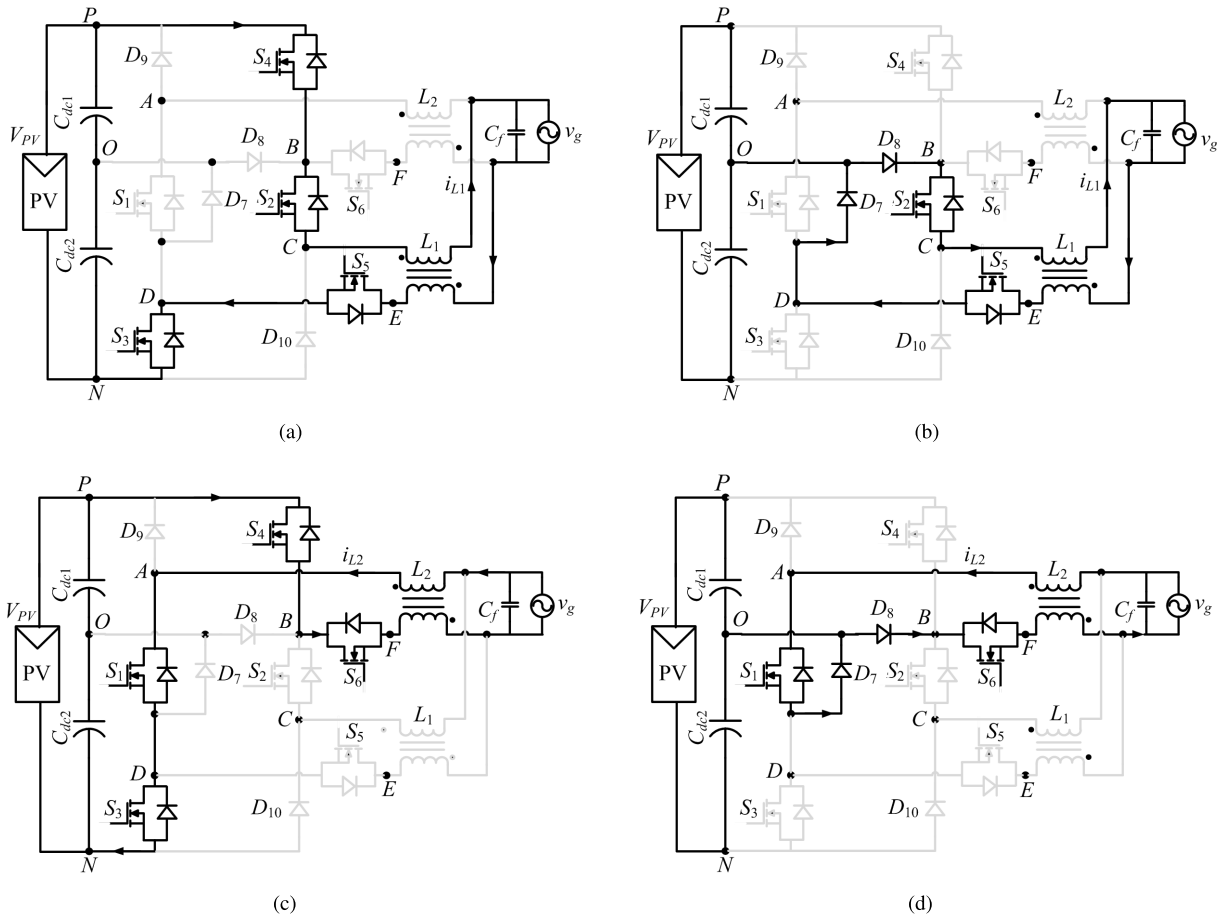

Fig. 3. Modes of operation of NIIFBC. (a) Powering mode in positive half-grid cycle. (b) Freewheeling mode in positive half-grid cycle. (c) Powering mode in negative half-grid cycle. (d) Freewheeling mode in negative half-grid cycle.

III. Analysis of the Superjunction MOSFET-Based NIIFBC

A. Description of NIIFBC Power Circuit

The power stage of the proposed superjunction MOSFET single-phase NIIFBC is depicted in Fig. 2(b). The topological derivation of this inverter is presented in [31]. Its both the phase legs come across the dc link through either coupled inductor L_1 or coupled inductor L_2. Hence, the possibility of shoot-through due to gate drive circuit failures is reduced, thereby improving its reliability. A hybrid SPWM switching strategy for the proposed inverter operating at UPF is depicted in Fig. 2(c). The control signal υ_{cont}, which is in phase with the rectified grid voltage, is referred to as a modulating signal. υ_{gs1} to υ_{gs6} are the gate-to-source control signals of power switches S_1 to S_6, respectively. Here, S_3 and S_4 are modulated at switching frequency over the complete grid cycle. The coupled filter inductor, L_1 is energized via S_2 and S_5 during positive half-grid cycles. On the other hand, L_2 is energized via S_1 and S_6 during negative half-grid cycles. During freewheeling periods, silicon carbide (SiC) diodes D_7 and D_8 maintain CMV at a constant value without causing reverse recovery loss in S_3 and S_4. Omission of diodes D_9 and D_{10} has no effect on the performance of the proposed inverter operating at UPF. However, they are useful when NIIFBC is operating at nonUPF. Four distinct operating modes of NIIFBC over a grid cycle are shown in Fig. 3. The dc link and grid voltages are denoted by V_{PV} and υ_g, respectively.

B. Operating Modes of Proposed NIIFBC

1) Operating Modes During Positive Half of the Grid Cycle:

a) Mode I (Powering Mode): The coupled inductor L_1 is energized through S_4, S_2, S_5, and S_3, and PV power is injected into grid. The path for the grid current is denoted by arrows, as depicted in Fig. 3(a). In this mode, the voltages at nodes C, B, E, and D with reference to N are V_{PV}, V_{PV}, zero, and zero, respectively. Thus, $\upsilon_{\text{CM}} = ((\upsilon_{\text{BN}} + \upsilon_{\text{DN}})/2) = (V_{\text{PV}}/2)$ and the differential mode voltage is $\upsilon_{\text{DM}} = \upsilon_{\text{BN}} - \upsilon_{\text{DN}} = V_{\text{PV}}$. The voltage stress on S_1 and S_6 is found using the mesh analysis, which is $\upsilon_{\text{DS1}} = \upsilon_{\text{DS6}} = ((V_{\text{PV}} + \upsilon_g)/2)$. Mode transition is initiated when gate signals to S_3 and S_4 are withdrawn.

b) Mode II (Freewheeling Mode): The PV source is disconnected from the grid when S_3 and S_4 are turned OFF. As a result, the grid current freewheels through S_5, D_7, D_8, S_2, L_1, and the grid, as illustrated in Fig. 3(b). The voltages at nodes C, B, E, and D with respect to N are clamped at $(V_{\text{PV}}/2)$, and $\upsilon_{\text{CM}} = ((\upsilon_{\text{BN}} + \upsilon_{\text{DN}})/2) = (V_{\text{PV}}/2)$. Thus, the differential mode voltage $\upsilon_{\text{DM}} = \upsilon_{\text{BN}} - \upsilon_{\text{DN}} = 0$. The voltage stress on S_1 and S_6 and that on S_3 and S_4 are $\upsilon_{\text{DS1}} = \upsilon_{\text{DS6}} = (\upsilon_g/2)$ and $\upsilon_{\text{DS3}} = \upsilon_{\text{DS4}} = (V_{\text{PV}}/2)$, respectively.

2) Operating Modes During Negative Half of the Grid Cycle:

a) Mode I (Powering Mode): In this mode, the coupled inductor L_2 is energized through S_4, S_6, S_1, and S_3. The PV power is injected into grid, and Fig. 3(c) illustrates the path for the grid current. $v_{\rm FN} = v_{\rm BN} = V_{\rm PV}$, $v_{\rm AN} = v_{\rm DN} = 0$, and $v_{\rm CM} = (V_{\rm PV}/2)$. The differential mode voltage $v_{\rm DM} = V_{\rm PV}$. The voltage stress on S_2 and S_5 is $v_{\rm DS2} = v_{\rm DS5} = ((V_{\rm PV} + v_g)/2)$. When the gate signals to S_3 and S_4 are withdrawn, the mode transition is initiated.

b) Mode II (Freewheeling Mode): In this mode, the PV source is disconnected from the grid. The freewheeling path for the grid current is depicted in Fig. 3(d). The diodes D_7 and D_8 clamp $v_{\rm BN}$, $v_{\rm AN}$, $v_{\rm FN}$, and $v_{\rm DN}$ at $(V_{\rm PV}/2)$. Therefore, $v_{\rm CM} = (V_{\rm PV}/2)$ and $v_{\rm DM} = 0$. The voltage stress on S_2 and S_5 is $v_{\rm DS2} = v_{\rm DS5} = (v_g/2)$ and that on S_3 and S_4 is $(V_{\rm PV}/2)$.

The following observations are elicited from Section III-B:

1) the loop CMV of conducting paths is maintained at a constant value of $(V_{\rm PV}/2)$ during positive and negative half-grid cycles, respectively;
2) the maximum voltage stress on S_3 and S_4 is $(V_{\rm PV}/2)$ and on S_1, S_2, S_5, and S_6 is $((V_{\rm PV} + V_g)/2)$, where V_g is the peak value of the grid voltage;
3) since S_1 and S_5 and S_2 and S_6 come across the grid through L_1 and L_2, the possibility of grid shoot-through at zero crossings is obviated;
4) no dead time is required during mode transitions.

C. Analysis of Ground Loop Leakage Current in NIIFBC

Although L_1 and L_2 are not energized during negative and positive half-grid cycles, respectively, the leakage current due to their loop CMV cannot be neglected. Hence, the loop CMVs of L_1 and L_2 when they are not energized are analyzed in this section. Various paths through which the leakage current flows are shown in Fig. 4(a). L_{1C} and L_{1E} and L_{2A} and L_{2F} are the self-inductances of the coupled inductors L_1 and L_2, respectively. The self-inductances of L_1 and L_2 are equal for adeptly designed magnetic circuits. $C_{\rm PV}$ denotes the equivalent stray capacitance of the PV source. The variation of voltage at nodes A, C, E, and F with respect to N is shown in Fig. 4(a).

During positive half-grid cycles, the potentials at nodes C and E are the same as B and D, respectively, as shown in Fig. 4(b). The generalized leakage current model for each path is shown in Fig. 4(c). Here, $v_{\rm CM1}$ and $v_{\rm CM2}$ are the loop CMVs of L_1 and L_2, respectively, and given as

$$v_{\rm CM1} = \frac{v_{\rm BN} + v_{\rm DN}}{2} \tag{18}$$

$$v_{\rm CM2} = \frac{v_{\rm AN} + v_{\rm FN}}{2} \tag{19}$$

where $v_{\rm AN}$, $v_{\rm FN}$, $v_{\rm BN}$, and $v_{\rm DN}$ are the voltages at nodes A, F, B, and D with respect to N, respectively. During the powering modes, $v_{\rm AN} = v_{\rm DS1}$ and $v_{\rm FN} = v_{\rm BN} - v_{\rm DS6}$. From the Section III-B, it is evident that $v_{\rm DS1}$ and $v_{\rm DS6}$ are equal to $((V_{\rm PV} + v_g)/2)$ and $v_{\rm BN}$ is equal to $V_{\rm PV}$. Hence, $v_{\rm CM2}$ can be

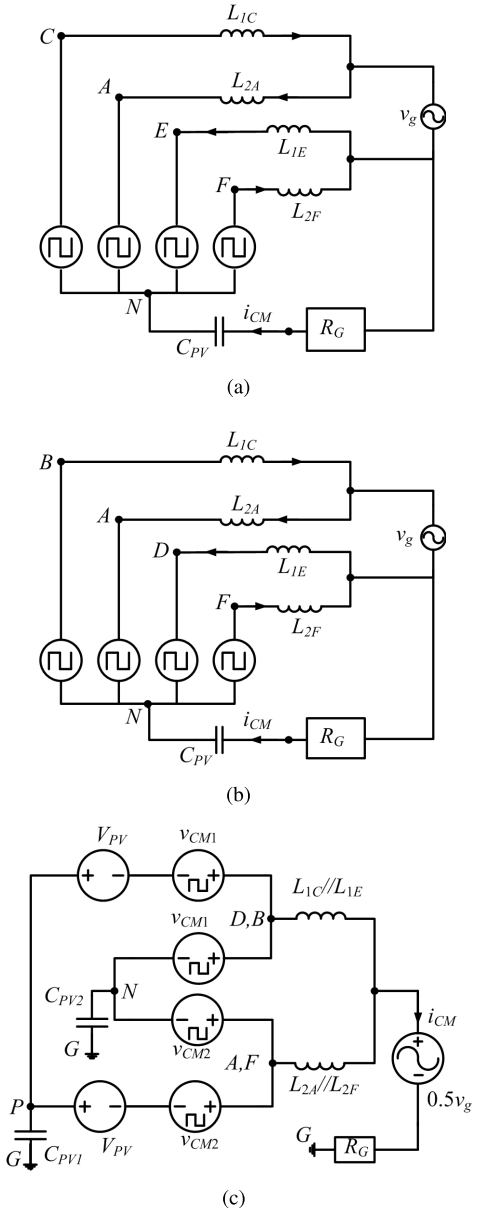

Fig. 4. (a) Paths for the flow of leakage current in NIIFBC. (b) Paths for the flow of leakage current in NIIFBC during positive half-grid cycle. (c) Generalized leakage current model of NIIFBC during positive half-grid cycle.

given as

$$v_{\rm CM2} = \frac{\frac{V_{\rm PV}+v_g}{2} + V_{\rm PV} - \frac{V_{\rm PV}+v_g}{2}}{2} = \frac{V_{\rm PV}}{2}. \tag{20}$$

During freewheeling modes, $v_{\rm AN}$ and $v_{\rm FN}$ are equal to $v_{\rm DS1} + v_{\rm DN}$ and $v_{\rm BN} - v_{\rm DS6}$, respectively. From the Section III-B, $v_{\rm DS1}$ and $v_{\rm DS6}$ are equal to $(v_g/2)$, and $v_{\rm DN}$ and $v_{\rm BN}$ are equal to $(V_{\rm PV}/2)$. Hence, $v_{\rm CM2}$ is evaluated as

$$v_{\rm CM2} = \frac{\frac{V_{\rm PV}+v_g}{2} + \frac{V_{\rm PV}-v_g}{2}}{2} = \frac{V_{\rm PV}}{2}. \tag{21}$$

From (20) and (21), it is worthwhile to comment that $v_{\rm CM2}$ is maintained at $(V_{\rm PV}/2)$ during positive half-grid cycles. Using the same approach mentioned above, it can be proved

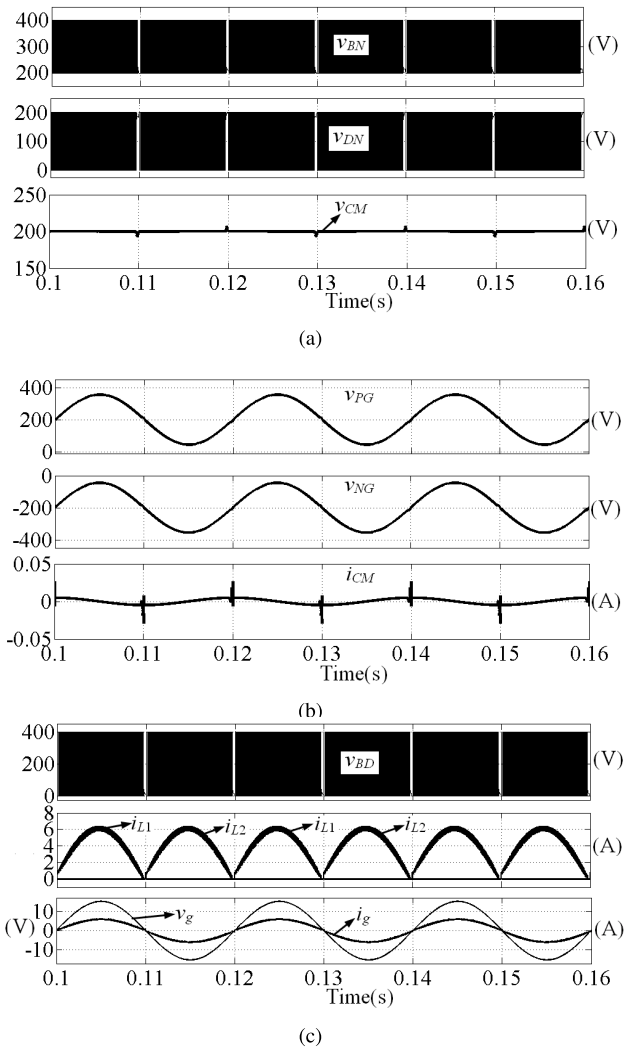

Fig. 5. Simulation results of NIIFBC. (a) Variation of $v_{\rm BN}, v_{\rm DN}$ and CMV ($v_{\rm CM}$). (b) Variation of voltage across PV stray capacitors ($v_{\rm PG}$ and $v_{\rm NG}$) and leakage current ($i_{\rm CM}$). (c) Variation of differential mode voltage ($v_{\rm BD}$), inductor currents (i_{L1} and i_{L2}), and grid current (i_g).

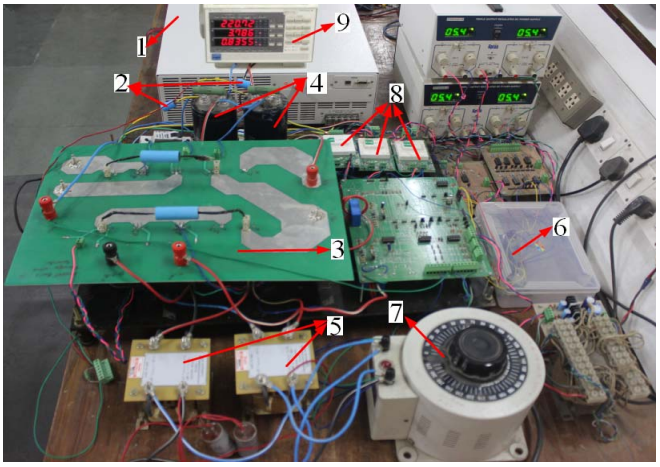

Fig. 6. Photograph of experimental setup. 1—variable dc voltage source. 2—PV stray capacitors ($C_{\rm PV1}$ and $C_{\rm PV2}$). 3—NIIFBC power circuit (see Fig. 2). 4—dc link split capacitors ($C_{\rm dc1}$ and $C_{\rm dc2}$). 5—coupled inductors (L_1 and L_2). 6—TMS320F28335 DSC. 7—utility grid. 8—gate drivers. 9—digital power analyzer (WT230).

TABLE I
SPECIFICATION AND POWER STAGE DEVICES FOR THE NIIFBC PROTOTYPE CIRCUIT

Parameter	Values
Rated power	1 kW
Input voltage	400 V
Grid voltage/frequency	220 V/50 Hz
Switching frequency (f_s)	20 kHz
Filter inductor L_1, L_2	2X1.5 mH
Filter capacitor C_f	2 μF
S_1, S_2, S_5, S_6	SPW55N80C3, super-junction MOSFET (800 V)
S_3, S_4	IPW60R045CP, super-junction MOSFET (600 V)
D_7, D_8, D_9, D_{10}	IDW20G65C5, SiC diodes (650 V)
D_7, D_8	APT30DQ60BG, soft recovery diodes
DC link capacitor C_{DC1}, C_{DC2}	940 μF
PV stray capacitor C_{PV1}, C_{PV2}	0.1 μF

that $v_{\rm CM1}$ remains at $(V_{\rm PV}/2)$ during negative half-grid cycles. As a result, $v_{\rm CM1}$ and $v_{\rm CM2}$ are maintained at $(V_{\rm PV}/2)$ for the complete grid cycle. Replacing $v_{\rm CM}$ by $(V_{\rm PV}/2)$ in (15) and (16) and neglecting the voltage drop due to $i_{\rm CM}$, the voltage across $C_{\rm PV1}$ and that across $C_{\rm PV2}$ are given by

$$v_{\rm PG} = \frac{V_{\rm PV} + v_g}{2} \tag{22}$$

$$v_{\rm NG} = \frac{-V_{\rm PV} + v_g}{2}. \tag{23}$$

Substituting (22) and (23) in (17), the leakage current as a function of v_g is given as

$$i_{\rm CM} = C_{\rm PV}\frac{d(v_g)}{dt}. \tag{24}$$

The peak value of leakage current can be obtained as

$$I_{\rm CM} = j\omega C_{\rm PV} V_g \tag{25}$$

where ω is the angular frequency of the grid voltage. For the given PV stray capacitance and grid voltage, the minimum leakage current, which a nonisolated full-bridge NPC inverter can generate, is given in (24). The proposed inverter with a constant CMV is also anticipated to evince a similar leakage current performance.

IV. Simulation and Experimental Validation of NIIFBC

A. Simulation Analysis

In order to validate the claims of the proposed inverter, simulation studies are carried out on a 1-kW NIIFBC circuit using MATLAB/Simulink software. The parameters used for these studies are as follows: the input voltage $V_{\rm PV}$ is 400 V, the grid voltage V_g is 220 V (rms), the switching frequency f_s is 20 kHz, coupled filter inductances L_1 and L_2 are 2×1.5 mH, the filter capacitance C_f is 2 μF, and PV stray capacitances $C_{\rm PV1}$ and $C_{\rm PV2}$ are 0.1 μF. The hybrid SPWM switching strategy for the proposed inverter operating at UPF operation is shown in Fig. 2(c). The dead time between the control signals is set to zero. In order to de-energize L_1 completely before energizing L_2 and vice-versa, S_3 and S_4 are turned OFF near the zero crossings of the grid voltage. $v_{\rm AN}$, $v_{\rm FN}$, $v_{\rm CN}$, and $v_{\rm EN}$ are the voltages at nodes A, F, C, and E with respect to N,

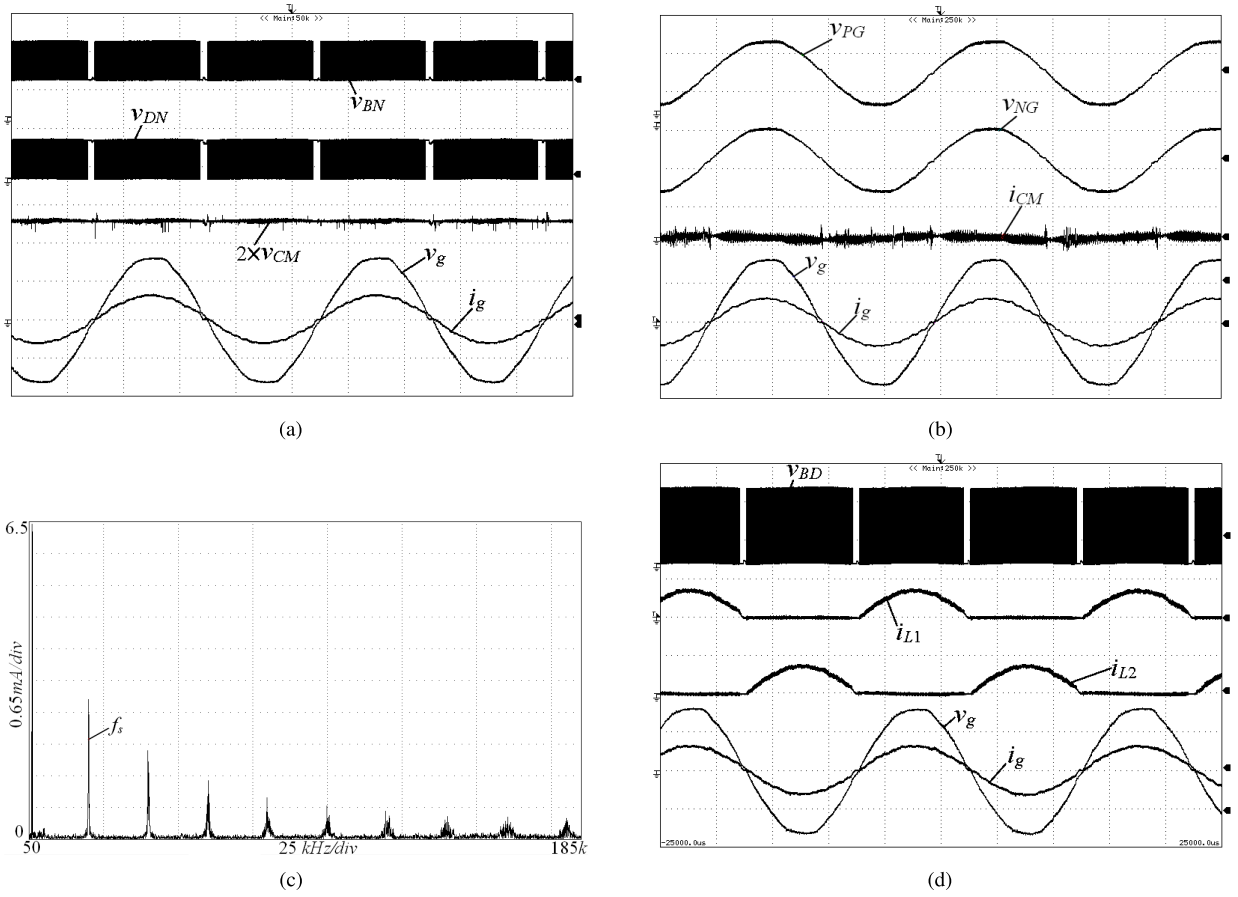

Fig. 7. Experimental results of NIIFBC: v_{BN}, v_{DN}, v_{BD}, v_{PG}, v_{NG}, and v_g (200 V/div); v_{CM} (50 V/div); i_g, i_{L1}, and i_{L2} (10 A/div); i_{CM} (0.2 A/div); and time scale: 5 ms/div. (a) Waveforms of v_{CM}, v_{BN}, and v_{DN}. (b) Waveforms of leakage current (i_{CM}), v_{PG}, and v_{NG}. (c) Harmonic spectrum of i_{CM}. (d) Waveforms of v_{BD} and inductor currents i_{L1} and i_{L2}.

respectively, as shown in Fig. 4(a). v_{AN} and v_{CN} are the same as v_{DN} and v_{BN} during positive and negative half-grid cycles, respectively. Therefore, v_{BN} and v_{DN} are measured to evaluate the CMV of NIIFBC.

Simulation waveforms of v_{BN} and v_{DN} along with v_{CM} are shown in Fig. 5(a). It is evident from Fig. 5(a) that the v_{CM} remains constant at $(V_{PV}/2)$ over the grid cycle. As a result, the voltages across the PV stray capacitors C_{PV1} and C_{PV2} vary at the grid frequency. Hence, the proposed inverter alleviates i_{CM} effectively. These facts are verified by the simulation waveforms of v_{PG}, v_{NG}, and i_{CM}, and they are shown in Fig. 5(b). The simulation waveforms of differential mode voltage (v_{BD}), filter inductor currents (i_{L1} and i_{L2}), and grid current (i_g) are shown in Fig. 5(c). Due to its circuit topology, v_{BD} of the proposed inverter varies between V_{PV} and zero over the grid cycle. L_1 and L_2 are energized during positive and negative half-grid cycles, respectively, and the current flowing through them is always positive, as shown in Fig. 5(c).

B. Experimental Validation

A 1-kW experimental prototype of NIIFBC is developed to validate the simulation results, shown as in Fig. 6. The power devices listed in Table I are used to fabricate the prototype. A variable dc source and two capacitors (0.1 μF and 1000 V) of polypropylene type are used for emulating the PV source to simplify the experimental study [25]. The efficiency of the proposed inverter is measured using a precision power analyzer (WT230) from Yokogawa. TMS320F28335 DSC from Texas Instruments is used to implement the phase-locked loop and the grid current control algorithms.

The variation of CMV is shown in Fig. 7(a). From Fig. 7(a), it is evident that v_{BN} and v_{DN} vary between V_{PV} and $(V_{PV}/2)$ and $(V_{PV}/2)$ and zero, respectively, without any overshoots. Therefore, the CMV is maintained at a constant value of $(V_{PV}/2)$ over the grid cycle. Further, the experimental results of v_g and i_g are in phase with each other. These waveforms demonstrate the UPF operation of the proposed inverter.

Fig. 7(b) shows the measured leakage current (i_{CM}) and voltages across the PV stray capacitors C_{PV1} (v_{PG}) and C_{PV2} (v_{NG}), respectively. v_{PG} and v_{NG} vary at grid frequency as the CMV is maintained at a constant value of $(V_{PV}/2)$. Thus, the experimental results comply with analytical relationships given in (22) and (23). Consequently, the i_{CM} is profiled by the grid voltage according to (17) and shown in Fig. 7(b). The harmonic spectrum of the leakage current is shown in Fig. 7(c). The measured values of the leakage current at grid and switching frequencies are 6.4 and 3.0 mA,

respectively. Furthermore, the rms value of i_{CM} is 7.6 mA. Thus, the leakage current generated by the NIIFBC is well below the German standard, VDE0126-1-1 limits.

The current flowing through L_1 and that through L_2 are shown in Fig. 7(d). Since they are energized during positive and negative half-grid cycles, they carry grid current for half a cycle only. This ensures that the body diode of each superjunction MOSFET switch is not activated. The gate-to-source control signals of S_3 and S_4 near the grid voltage zero crossings are deliberately withdrawn to de-energize L_1 and L_2 completely. As a result, a small deviation in i_g is observed near the zero crossings of the grid voltage.

The variation of voltage across S_1 to S_6 is shown in Fig. 8(a). The maximum voltage across S_3 and S_4 is $(V_{PV}/2)$. However, the voltage across S_1 and S_6 and that across S_2 and S_5 vary between $((V_{PV}+v_g)/2)$ and $(v_g/2)$ during positive and negative half cycles of the grid voltage, respectively. This fact is evident from Fig. 8(a) and confirms the theoretical analysis presented in Section III-B. Thus, the veracity of the leakage current analysis presented in Section III-C is verified experimentally. The input voltage is uniformly distributed between the dc link split capacitors C_{dc1} and C_{dc2}, as shown in Fig. 8(b). This is achieved by connecting a 100-kΩ resistor across each dc link split capacitor, which results in negligible loss. As a result, the CMV is clamped at $(V_{PV}/2)$ during the freewheeling periods.

The measured efficiencies of the proposed inverter at different load conditions with the dc link voltage of 400 V are shown in Fig. 8(c). The measured efficiencies do not incorporate power loss into gate drivers and the sensing circuit. The proposed inverter with SiC external diodes has the peak efficiency of 98.8%. On the other hand, its peak efficiency with ultrafast soft recovery diodes is 98%. The measured efficiencies at different power levels with weighted factors are added according to (26) to evaluate the EU efficiency of NIIFBC as

$$\eta_{EU} = 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%}. \quad (26)$$

The evaluated EU efficiencies of NIIFBC with SiC and ultrafast soft recovery diodes are 98.3% and 97.7%, respectively. Therefore, the low leakage current, high EU efficiency, and enhanced reliability claims of the proposed inverter with SiC external diodes are validated experimentally.

V. Performance Comparison with Existing Topologies

A. Total Power Loss Estimation of Semiconductor Devices

The total power loss of semiconductor devices in the proposed inverter is calculated based on the specifications listed in Table I. The piecewise linear ON-state voltage models of superjunction MOSFET (v_{ds}) and diode (v_{ak}) are given as

$$\text{MOSFET: } v_{ds} = i_L R_{ds} \quad (27)$$

$$\text{SiC diode: } v_{ak} = V_f + i_L R_{ak} \quad (28)$$

where R_{ds} and R_{ak} are their ON-state resistances, respectively. V_f is the forward voltage drop across diode when the current flowing through it is zero. These values are usually derived from their respective data sheets, as listed in Table I. The inductor current i_L is given by $i_L = I_L \sin(\omega t)$, where I_L is

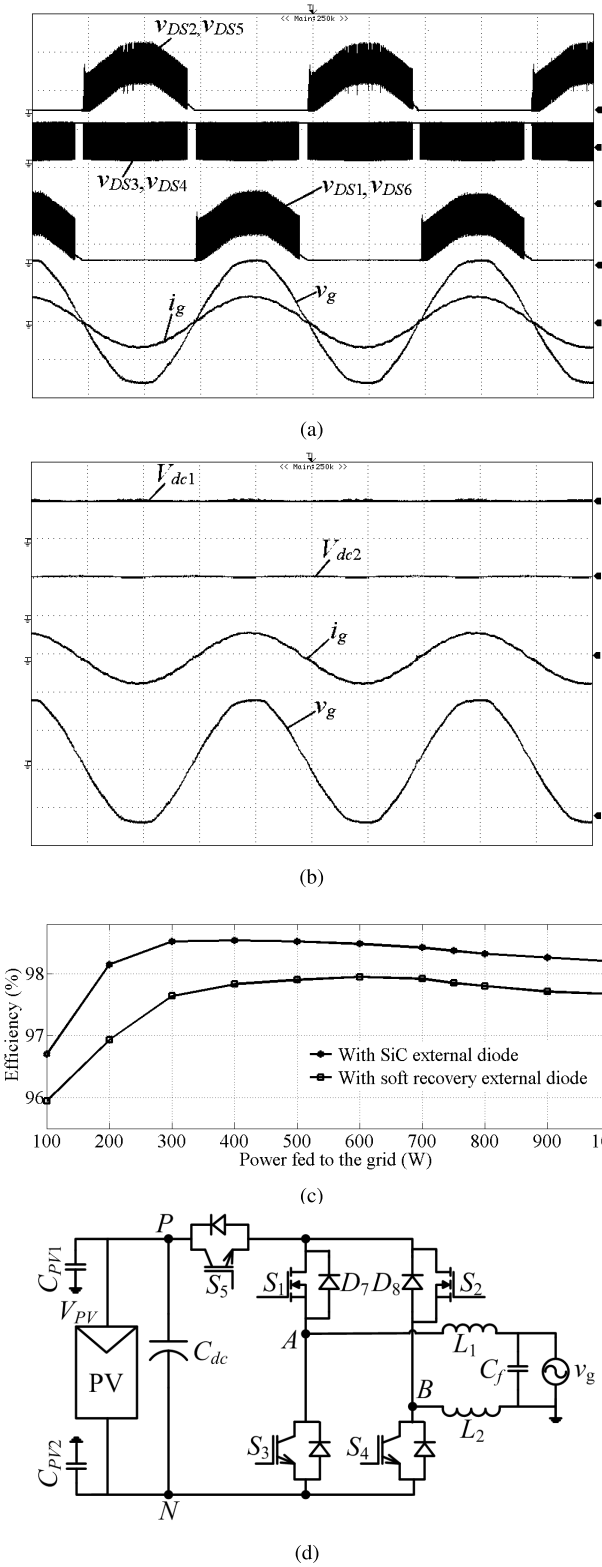

Fig. 8. (a) Measured voltage stress on devices of NIIFBC. $v_{DS1} - v_{DS6}$, v_g (200 V/div), i_g (10 A/div), and time scale: 5 ms/div. (b)Voltage distribution across dc link split capacitors. V_{dc1}, V_{dc2}, v_g (200 V/div), i_g (10 A/div), and time scale: 5 ms/div. (c) Measured efficiencies of NIIFBC at various loads. (d) H5 inverter topology.

its maximum value. In the case of continuous conduction mode, the powering and the freewheeling mode duty ratios are given by

$$d_{\text{pow}} = M\sin(\omega t) \tag{29}$$

$$d_{\text{free}} = 1 - M\sin(\omega t) \tag{30}$$

where M is the modulation index. Using (31) and (32), the conduction losses in S_3 and S_4 and D_7 and D_8 are computed, respectively, as

$$P_{\text{Cond}(S_3,S_4)} = \frac{1}{\pi}\int_0^{\pi} v_{\text{ds}} i_L d_{\text{pow}} d\omega t = I_L^2 R_{\text{ds}} \frac{4M}{3\pi} \tag{31}$$

$$P_{\text{Cond}(D_3,D_4)} = \frac{1}{\pi}\int_0^{\pi} v_{\text{ak}} i_L d_{\text{free}} d\omega t = I_L V_f\left(\frac{2}{\pi} - \frac{M}{2}\right) + I_L^2 R_{\text{ak}}\left(\frac{1}{2} - \frac{4M}{3\pi}\right). \tag{32}$$

Further, using (33), the conduction loss in S_1, S_2, S_5, and S_6 is computed as

$$P_{\text{Cond}(S_1,S_2,S_5,S_6)} = \frac{1}{2\pi}\int_0^{\pi} v_{\text{ds}} i_L d\omega t = \frac{I_L^2 R_{\text{ds}}}{4}. \tag{33}$$

The power loss also occurs in MOSFET during the turn-ON transitions due to the stored energy in junction capacitance and diode reverse recovery current (I_{rr}). The equivalent power loss due to discharge of the stored energy on the junction capacitance is evaluated as

$$P_{\text{MOS-OSS}} = E_{\text{oss}}(V_{\text{ds}}) f_s \tag{34}$$

where $E_{\text{oss}}(V_{\text{ds}})$ and f_s are the ON-state stored (OSS) energy loss in the junction capacitance of MOSFET and switching frequency, respectively. $E_{\text{oss}}(V_{\text{ds}})$ can be obtained from the data sheet of the superjunction MOSFETs that are listed in Table I. The power loss in the superjunction MOSFET due to diode I_{rr} is computed as [32]

$$P_{\text{MOS}(I_{\text{rr}})} = \left(\frac{I_L t_a}{\pi} + \frac{I_{\text{rr}}(2t_a + t_b)}{8}\right) V_{\text{PV}} f_s \tag{35}$$

where t_a and t_b are the parameters of reverse recovery time (t_{rr}). The power loss in ultrafast soft recovery diode during t_{rr} is given by [33], [34]

$$P_{\text{OFF-trans}} = \left(\frac{I_{\text{rr}} t_b}{3}\right) V_{\text{PV}} f_s. \tag{36}$$

However, power loss during the turn-OFF transitions is negligible in the SiC diode. On the other hand, the power loss due to the dissipation of stored energy in the junction capacitance of the SiC diode during turn-ON transition is computed as

$$P_{\text{SiCdiode-OSS}} = E_c(V_{\text{ak}}) f_s \tag{37}$$

where $E_c(V_{\text{ak}})$ is the stored energy loss in the junction capacitance of the SiC diode.

The total power loss in each semiconductor device of the NIIFBC is calculated by substituting the respective device parameters in (31) to (37) and compared with that of H5, H6, and high reliability and efficiency (HRAE) inverter topologies [15], [19], [22]. These topologies are considered for comparison purpose because of their excellent performance

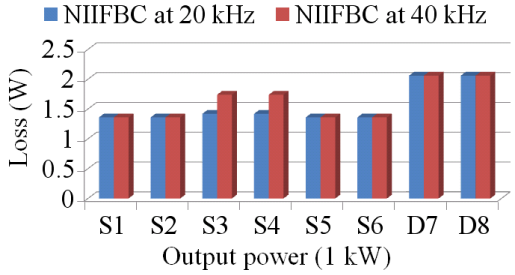

Fig. 9. Comparison of total power loss in semiconductor devices of NIIFBC at 20-kHz and 40-kHz switching frequencies.

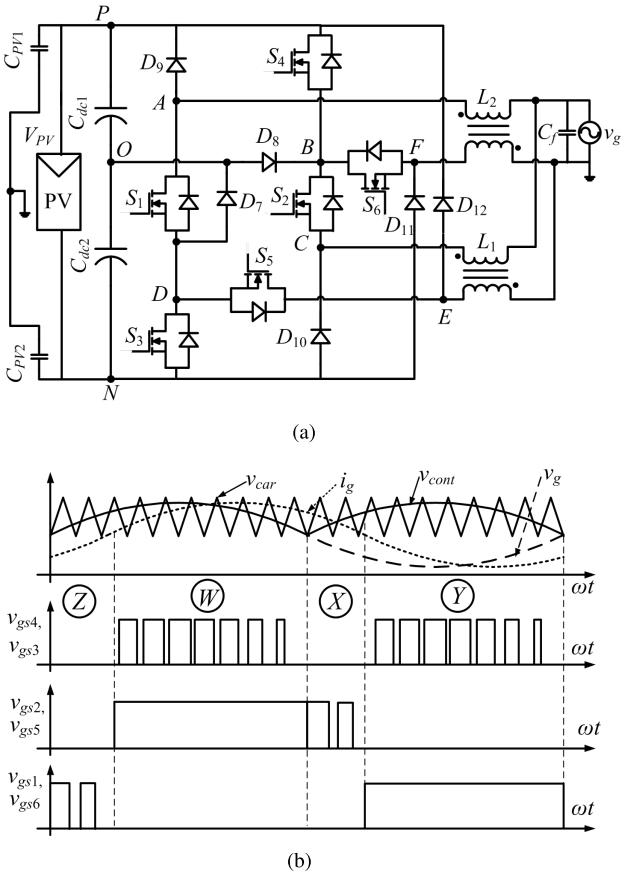

Fig. 10. (a) Circuit topology of VNIIFBC. (b) Hybrid SPWM switching strategy for VNIIFBC operating at non-UPF.

in terms of conversion efficiency. The circuit topology of H5 inverter is shown in Fig. 8(d). For a fair comparison, devices used in H5 inverter are listed in Table II. The total loss in each IGBT is estimated by substituting the respective device parameters in equations presented in [25]. The comparison of the total power loss in H5, H6, HRAE, and the proposed inverters at full load is made in Table III. The total power loss in the HRAE inverter is less than that in the others and is approximately equal to that in the H6 inverter. The total power loss in the NIIFBC is higher than that in the H5 inverter. However, the estimated total power loss in the NIIFBC with 650 V devices is 10.04 W, which is less than that in the H5 inverter. The power loss distribution among the semicon-

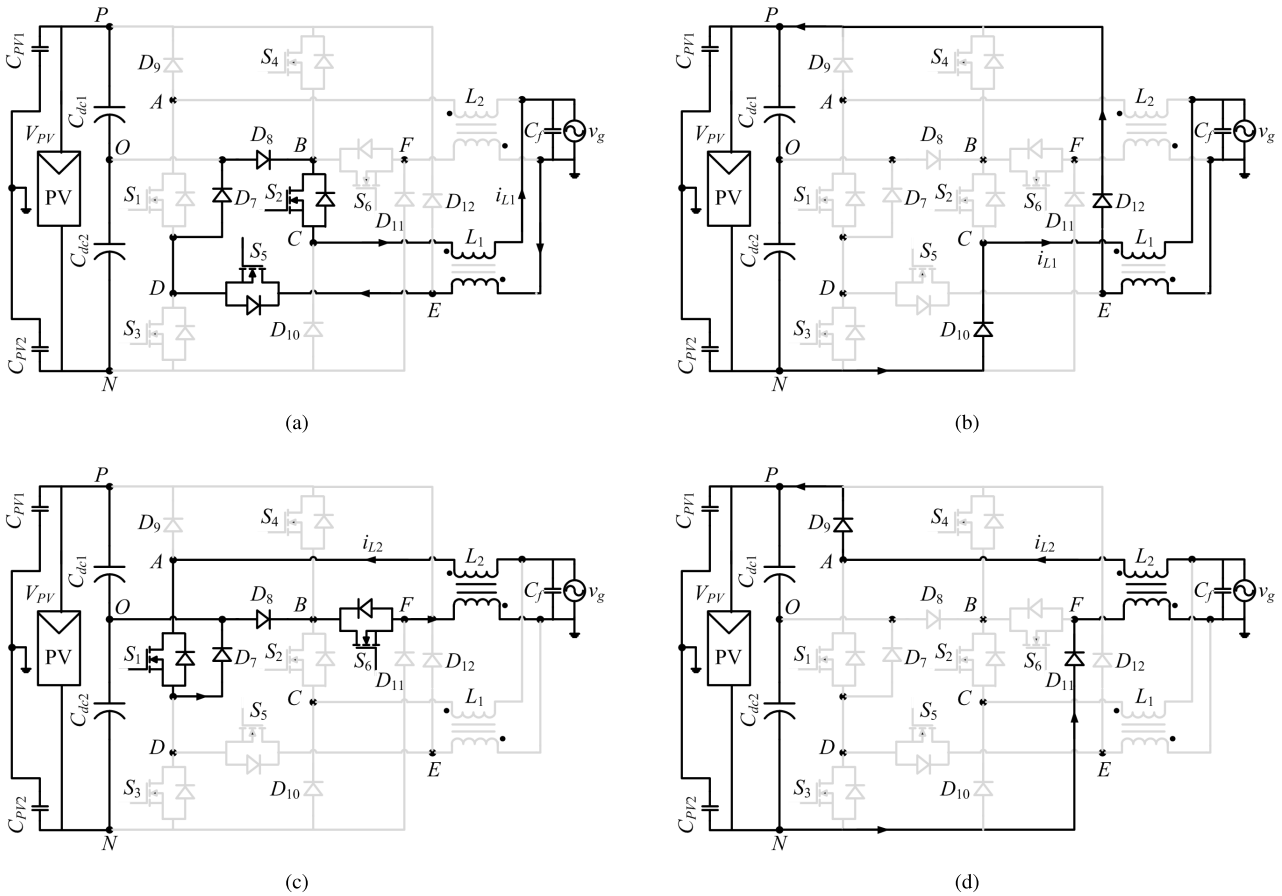

Fig. 11. Modes of operation of VNIIFBC supplying reactive power to grid. (a) and (b) Modes of operation in the region X. (c) and (d) Modes of operation in the region Z.

TABLE II
DEVICES USED IN H5 INVERTER

Device	Rating
S_1, S_2	IPW60R045CP, MOSFET (650 V)
S_3, S_4, S_5	IKW20N60T, IGBT (600 V)
D_7, D_8	IDW20G65C5, SiC diodes (650 V)

TABLE III
TOTAL POWER LOSS OF DEVICES AT RATED POWER

	H5 (W)	H6 (W)	HRAE (W)	NIIFBC (W)	NIIFBC with 650 V devices (W)
S_1	0.8	1.1	1.1	1.36	0.8
S_2	0.8	1.1	1.1	1.36	0.8
S_3	1.9	0.8	1.1	1.42	1.42
S_4	1.9	0.8	1.1	1.42	1.42
S_5	3.8	1.1	0.6	1.36	0.8
S_6	0	1.1	0.6	1.36	0.8
D_7	1.3	1.2	1.2	2.0	2.0
D_8	1.3	1.2	1.2	2.0	2.0
Total	11.8	8.4	8	12.3	10.04

Note: $V_{PV} = 400V$.

ductor devices of the NIIFBC operating at 20 and 40 kHz switching frequencies is depicted in Fig. 9. When the NIIFBC is operated at 40 kHz, only the power loss in S_3 and S_4 increases since they are controlled at switching frequency. The increment in the total power loss of S_3 and that of S_4 are small, as depicted in Fig. 9. Therefore, it is possible to have a compact design of the proposed inverter at higher switching frequencies.

B. Performance Evaluation

The performance comparison of the NIIFBC with the state-of-the-art nonisolated inverter topologies is listed in Table IV. The H6 inverter topology evinces poor performance in terms of the leakage current compared with others. In addition, it has the possibility of phase leg shoot-through as in H5 and FBDCBP inverter topologies. Such a limitation is reduced in HRAE and NIIFBC topologies. The proposed NIIFBC exhibits high EU efficiency next to the HRAE inverter. However, the leakage current and the device count in the HRAE inverter are higher than FBDCBP and NIIFBC topologies.

C. Reactive Power Compensation

The proposed inverter by its innate circuit structure cannot not supply reactive power to the grid. In order to incorporate this feature, its circuit structure is modified, as shown in Fig. 10(a). This circuit is referred as the variant of NIIFBC (VNIIFBC). The hybrid SPWM switching strategy

TABLE IV
PERFORMANCE COMPARISON OF NIIFBC WITH THE STATE-OF-THE-ART FULL-BRIDGE NPC TOPOLOGIES

Topology	Switch count	Diode count	Shoot-through limitation (excluding devices short-circuit)	Constant v_{CM}	i_{CM} at f_s	i_{CM} (RMS)	EU(%)
FBDCBP [27]	6	2	✓	✓	3 mA	-	96.4 [28]
H5	5	0	✓	X	6 mA [18]	-	96.7 [18]
H6	6	2	✓	X	-	45.8 mA [26]	98.2 [19]
HRAE	6	6	X	X	-	10.8 mA [22]	99 [22]
NIIFBC	6	4	X	✓	3 mA	7.6 mA	98.3

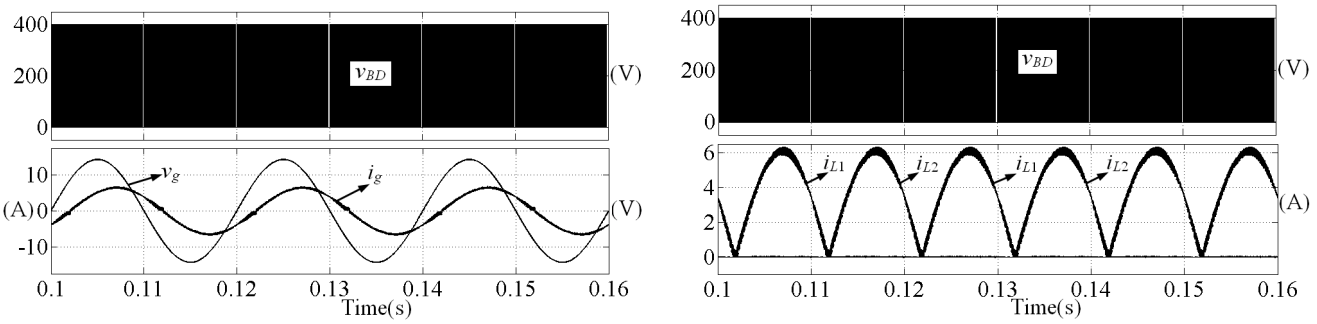

Fig. 12. Simulation results of the 1-kVA VNIIFBC circuit operating at 0.8 PF (lag). (a) Waveform of current fed to the grid.(d) Waveform of currents flowing through L_1 and L_2.

for VNIIFBC operating at nonUPF is depicted in Fig. 10(b). The control signal v_{cont} is in phase with the rectified grid voltage. Depending on the polarity of v_g and i_g, the modes of operation of VNIIFBC over a grid cycle are categorized into four regions, W, X, Y, and Z. The signals v_g and i_g have the same polarity in the regions of W and Y. The modes of operation of the VNIIFBC in these regions are identical to those depicted in Fig. 3. In order to avoid replication, only the circuit operations of the VNIIFBC in the X and Z regions are analyzed in the following.

1) Circuit Operation in X Region: In this region, v_g and i_g are negative and positive, respectively. S_5 and S_2 are modulated at switching frequency and the other switches are turned OFF. When S_2 and S_5 are turned ON, the grid voltage energizes L_1, as depicted in Fig. 11(a). The governing voltage relationships in this mode are $v_{\text{CN}} = v_{\text{EN}} = v_{\text{CM1}} = (V_{\text{PV}}/2)$, $v_{\text{CE}} = 0$, and $v_{\text{BD}} = 0$. Using the mesh analysis, $v_{\text{FN}}, v_{\text{AN}}$, and v_{CM2} are obtained as $((V_{\text{PV}} - v_g)/2)$, $((V_{\text{PV}} + v_g)/2)$, and $(V_{\text{PV}}/2)$, respectively. If S_2 and S_5 are turned OFF, the stored energy in L_1 is fed to the dc link through D_{10} and D_{12}. The equivalent circuit for this mode is depicted in Fig. 11(b). The governing voltage relationships in this mode are $v_{\text{CN}} = 0$, $v_{\text{EN}} = V_{\text{PV}}$, $v_{\text{CM1}} = (V_{\text{PV}}/2)$, and $v_{\text{CE}} = -V_{\text{PV}}$. The values of v_{FN}, v_{AN}, and v_{BD} are obtained using mesh analysis as V_{PV}, zero, and V_{PV}, respectively. Hence, the loop CMV of L_2 is given as $v_{\text{CM2}} = (V_{\text{PV}}/2)$.

2) Circuit Operation in Z Region: In this region, the signals v_g and i_g are positive and negative, respectively. The grid voltage energizes L_2 when S_1 and S_6 are turned ON. The equivalent circuit for this mode is depicted in Fig. 11(c). The voltage at A, B, D, and F with respect N are equal to $(V_{\text{PV}}/2)$, and hence $v_{\text{CM2}} = (V_{\text{PV}}/2)$ and $v_{\text{BD}} = 0$.

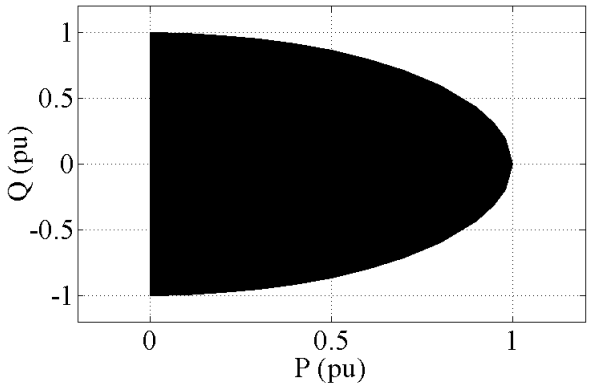

Fig. 13. Two-quadrant PQ operational area of VNIIFBC topology based on current limit.

The values of $v_{\text{CN}}, v_{\text{EN}}$, and v_{CM1} are obtained using mesh analysis as $((V_{\text{PV}} - v_g)/2)$, $((V_{\text{PV}} + v_g)/2)$, and $(V_{\text{PV}}/2)$, respectively. The stored energy in L_2 is fed to the dc link though D_9 and D_{11} when S_1 and S_6 are turned OFF, as shown in Fig. 11(d). The governing voltage relationships in this mode are $v_{\text{FN}} = 0$, $v_{\text{AN}} = V_{\text{PV}}$, $v_{\text{CM2}} = (V_{\text{PV}}/2)$, and $v_{\text{AF}} = V_{\text{PV}}$. Using mesh analysis, v_{CN}, v_{EN}, and v_{BD} are obtained as V_{PV}, zero and V_{PV}, respectively. Hence, the loop CMV of L_1 is given as $v_{\text{CM1}} = (V_{\text{PV}}/2)$.

Matalab/Simulink software is used to perform simulation studies on a 1-kVA VNIIFBC circuit operating at 0.8 PF (lag). The simulation results that validate the non-UPF operation of the circuit are shown in Fig. 12. A two-quadrant PQ operational area of the VNIIFBC circuit based on current limit is shown in Fig. 13. The polarity of the active power P injected

from the dc side to the grid is denoted by positive. However, the active power from the grid to the dc side cannot be injected due to the presence of uncontrolled devices D_7 and D_8.

VI. Conclusion

In this paper, a superjunction MOSFET-based NIIFBC is proposed. Its circuit structure reduces the possibility of shoot-through at switching frequency and improves the reliability of the grid-tied PV system. It interfaces the PV source to the grid through coupled filter inductors L_1 and L_2 during positive and negative half-grid cycles, respectively. As a result, there is no possibility of reverse recovery loss in main switches due to their body diodes. During freewheeling periods, the SiC diodes of NIIFBC clamp CMV at a constant value and do not cause reverse recovery loss in main switches. Hence, the authors claim that the proposed inverter can attain high EU and high energy conversion efficiencies. Furthermore, its low leakage current feature is analyzed and confirmed using a new generalized leakage current model presented in this paper. In order to ascertain the above claims of NIIFBC and the veracity of the generalized leakage current model, experimental studies are carried out on a 1-kW prototype circuit. The experimental results are supportive of the theoretical claims made for the NIIFBC, as in the following ways:

1) it reduces the possibility of shoot-through at switching frequency, which improves the reliability of the grid-tied PV system;
2) improved quality of current injected into the grid, as no dead time is required at grid voltage zero crossings;
3) the high EU and peak efficiencies of 98.3% and 98.8%, respectively;
4) low leakage current that complies with the German standard, VDE0126-1-1;
5) superior differential mode characteristics;
6) superior overall performance compared with the state-of-the-art nonisolated full-bridge inverter topologies.

In order to supply the reactive power to the grid, a variant circuit of NIIFBC (VNIIFBC) is proposed. The simulation results that confirm the non-UPF operation of VNIIFBC are presented. Hence, the variant circuit of the proposed inverter is a promising solution for the grid-tied single-phase nonisolated PV system.

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